AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claim 12.

1. (Previously Presented) An apparatus comprising:

a buffer circuit to control the transition rate on an output pad of the buffer circuit;

a first amplifier having an input terminal and an output terminal, the output terminal coupled to the output pad;

a feedback component to couple feedback current from the output pad to the input terminal; and

a current mirror to multiply effects of the feedback current on the input terminal without increasing the feedback current through the feedback component.

2. (Previously Presented) The apparatus of claim 1, wherein the feedback component comprises a capacitor.

3. (Previously Presented) The apparatus of claim 1, wherein the current mirror comprises a second amplifier electrically connected to conduct a first current directly proportional to the feedback current.

4. (Previously Presented) The apparatus of claim 1, wherein the current mirror comprises

a second amplifier having a first sourc terminal, a first drain terminal and a first gate terminal; and

a third amplifier having a second source terminal, a second drain terminal and a second gate terminal, the first gate terminal and the second gate terminal are electrically connected, and the first drain couples to the feedback component.

5. (Previously Presented) The apparatus of claim 2, wherein the capacitor is a folded capacitor.

6. (Previously Presented) The apparatus of claim 1, wherein the apparatus comprises a Universal Serial Bus low-speed output circuit.

7. (Previously Presented) The apparatus of claim 1, wherein the current mirror possess a gain greater than one.

8. (Previously Presented) A controlled slew rate buffer circuit, comprising:

a capacitor coupled between an output terminal of the buffer circuit and a input terminal of a first driver amplifier; and

a first current mirror coupled to the capacitor and between the input terminal and the output terminal.

9. (Previously Presented) The buffer circuit of claim 8, wherein the first current mirror to increase feedback current at the input terminal independent of increasing the actual current flowing through the capacitor.

10. (Previously Presented) The buffer circuit of claim 8, further comprising:

a second driver amplifier to pull-up voltage level on the output terminal,a second current mirror possessing a first gain, the second current mirror couples to the second driver; and

the first driver amplifier to pull-down voltage level on the output terminal, the first current mirror possessing a second gain, the second gain having a different value than the first gain.

11. (Previously Presented) The buffer circuit of claim 8, wherein the buffer circuit comprises a Universal Serial Bus low-speed output circuit.

12. (Currently Amended) The buffer circuit of claim 8, further comprising:

a pre-driver amplifier coupled to ~~between~~ the capacitor and the first driver amplifier.

13. (Previously Presented) The buffer circuit of claim 8, further comprising:

pull-up circuitry to generate a first slew rate at the output terminal for pulling up the voltage on the output terminal; and

pull-down circuitry to generate a second slew rate at the output terminal for pulling down the voltage on the output terminal.

14. (Previously Presented) A method, comprising:

controlling impedance of an output stage to obtain a predetermined rate of change of voltage at the output stage through use of capacitive fe dback between the output stage and a pre-driver circuit; and

mirroring current flow through the capacitive feedback and then multiplying the mirrored current flow.

15. (Previously Presented) The method of claim 14, further comprising:

multiplying effects of the capacitive feedback on the pre-driver circuit in order to decrease a capacitance value of a feedback capacitor used to achieve the predetermined rate of change of voltage.

16. (Previously Presented) The method of claim 14, further comprising:

generating a first slope for the predetermined rate of change of voltage at the output stage for pulling up voltage on the output stage; and

generating a second slope for the predetermined rate of change of voltage at the output stage for pulling down voltage on the output stage, the second slope having a different value than the first slope.

17. (Previously Presented) An apparatus, comprising:

means for controlling impedance of an output stage to obtain a predetermined rate of change of voltage at the output stage through use of capacitive feedback between the output stage and a pre-driver circuit; and

means for mirroring current flow through the capacitive feedback and then multiplying the mirrored current flow.

18. (Previously Presented) The apparatus of claim 17, further comprising:

means for multiplying effects of the capacitive feedback on the pre-driver circuit in order to decrease a capacitance value of a feedback capacitor used to achieve the predetermined rate of change of voltage.

19. (Previously Presented) The apparatus of claim 17, further comprising:

means for generating a first slope for the predetermined rate of change of voltage at the output stage for pulling up voltage on the output stage; and

means for generating a second slope for the predetermined rate of change of voltage at the output stage for pulling down voltage on the output stage, the second slope having a different value than the first slope.

20-23. Canceled

24. (Previously Presented) An apparatus, comprising:

an impedance controller to obtain a predetermined rate of change of voltage at an output stage through use of capacitive feedback between the output stage and a pre-driver circuit; and

a current mirror to multiply the effects of the capacitive feedback on the pre-driver circuit in order to decrease a capacitance value of a feedback capacitor used to achieve the predetermined rate of change of voltage.

25. (Previously Presented) The apparatus of claim 24, further comprising:

a first driver amplifier to generate a first slope for the predetermined rate of change of voltage at the output stage for pulling up voltage on the output stage; and

a second driver amplifier to generate a second slope for the predetermined rate of change of voltage at the output stage for pulling down voltage on the output stage, the second slope having a different value than the first slope.

26. (Previously Presented) The apparatus of claim 24, wherein the current mirror further comprises a programmable variable gain current mirror.